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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/494,953	02/01/2000	Yoshiharu Kato	P8075-9034	4157

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Arent Fox Kintner Plotkin & Kahn PLLC
1050 Connecticut Avenue NW
Suite 600
Washington, DC 20036-5339

EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	11

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,953	KATO, YOSHIHARU	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to amended claims 11-14, 18-21 and 26-30 and previously examined claims 1-10, 15-17, 22-25 and 31-48 filed March 21, 2003 have been fully considered but they are not persuasive.

The Applicant contends, "Applicant respectfully submits that each and every element recited within claims 18, 24, 25 and 30 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the test method and test circuit for an electronic device as recited in the present application is clearly distinct from that which is illustrated in JP '857. Specifically, it is respectfully submitted that JP '857 fails to disclose or suggest the limitation of a second semiconductor device inverting a first logical output signal and provides the first semiconductor device with an inverted signal (second logical output signal), and also fails to disclose or suggest the limitation of a test circuit that is activated in a test mode and is deactivated in a normal operation mode".

As per "JP '857 fails to disclose or suggest" ... "a second semiconductor device inverting a first logical output signal and provides the first semiconductor device with an inverted signal (second logical output signal)".

The Examiner asserts that claim 18 explicitly states, "wherein the first semiconductor device includes: a first output circuit connected to one of the bus lines for supplying the

bus line with a first logical output signal, an inversion output circuit connected to the bus lines for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal" and does not even indicate anywhere in the claim that the second semiconductor device has a means for "inverting a first logical output signal". The Examiner asserts that the inversion means in claim 1 exists on the first semiconductor circuit precisely as taught in JP '857.

Claim 24 explicitly states, "the second semiconductor device receives a first bus line signal and supplies a bus line with a second logical output signal being an inverted signal of the first bus line signal".

The Examiner asserts that claim 24 only claims that the second semiconductor device supplies a bus line with a second logical output signal precisely as taught in JP '857 and says absolutely nothing about "a second semiconductor device inverting a first logical output signal".

Claim 25 is similar to claim 18 in construction, in that the inversion output circuit is an element of the first semiconductor circuit not the second precisely as taught in JP '857. As such claims 18 and 25 demonstrate that the Applicant regards the circuit taught in JP '857 as an embodiment of a means for testing using the method taught in the Applicant's disclosure.

As per claim 30, claim 30 fails to even use any word related to invert or inversion anywhere in the claim.

As per "JP '857 fails to disclose or suggest" ... "the limitation of a test circuit that is activated in a test mode and is deactivated in a normal operation mode".
Claims 18, 24 and 25 fail to use words such as test mode, normal operation or anything related to such language.
The Examiner asserts that JP '857 teaches a test device for testing buses that are typically used to transmit data in normal mode. It is ridiculous to even think that testing can continue during normal operation without at the least deteriorating bandwidth and at worst obstructing communication. It is highly unlikely that test mode would continue during normal operation since, at the point in time that it is determined that the bus is operational, there is no need for the test to continue unless the designer is purposely trying to obstruct data flow. Finally, the title of the JP '857 patent is "Circuit for Testing Connection Between LSI". There is no indication that the circuit taught in the JP '857 patent has any value outside of testing.

The Applicant contends, "Applicant respectfully submits that each and every element recited within claims 1, 6, 11 and 47 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the test method and test circuit for an electronic device as recited in the present application is clearly distinct from that which is illustrated in JP `857. Specifically, it is respectfully submitted that JP '857 fails to disclose or suggest the limitation of a second semiconductor device inverting a first logical output signal and provides the first semiconductor device with an inverted signal (second logical output signal), and fails to

disclose or suggest the limitation of a clamp circuit that clamps respective input terminals to a specific potential".

As per "JP '857 fails to disclose or suggest the limitation of a second semiconductor device inverting a first logical output signal and provides the first semiconductor device with an inverted signal (second logical output signal)". The Examiner would like to point out that that the purpose of the claimed invention of the Applicant's claim 1 and the teachings of Akiyama is to compare an inverted version of a test signal transmitted on a line to test for connectivity. Placement of inverters to achieve this objective is an obvious Engineering Design choice as acknowledged by the Applicant in the Applicant's claim 18 which is an alternative embodiment of the invention claimed in the Applicant's claim 1 and which is substantially identical to the teachings in the Akiyama patent whereby the signal is inverted by the inversion circuit on the first semiconductor and supplied to the second semiconductor which in turn supplies the inverted signal to the first semiconductor for comparison.

Applicant's claim 6 explicitly cites, "the first semiconductor device generating a second logical output signal being an inverted signal of the first logical output signal and supplying the selected bus line with the second logical output signal" which is consistent with the JP '857 patent.

Applicant's claim 11 is similar in construction to claim 1 and the same arguments that applies to claim 1 also applies to claim 11.

As per claim 47, claim 47 fails to even use any word related to invert or inversion anywhere in the claim.

As per "JP '857 fails to disclose or suggest" ... "the limitation of a clamp circuit that clamps respective input terminals to a specific potential". The Examiner asserts that as cited clamping respective input terminals to a specific potential is a function of a latch circuit in order to isolate circuitry from the effect of interfacing. 6 and 7 in the JP '857 patent are latches. The Applicant's Figure 11 and 12 are also standard latch circuits. The Examiner asserts use of specific device to implement the design in the JP '857 patent do not deviate from the scope or the intent of the teachings in the JP '857 patent.

The Examiner disagrees with the applicant and maintains the rejection to amended claims 11-14, 18-21 and 26-30 and previously examined claims 1-10, 15-17, 22-25 and 31-48. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that amended claims 11-14, 18-21 and 26-30 and previously examined claims 1-10, 15-17, 22-25 and 31-48 as rejected below are not patentably distinct or non-obvious over the prior art of record in view of the reference, Akiyama, Hideki (JP 05053857 A) as applied in the last office action, Paper No. 8. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 18-21, 24-26, 28, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama, Hideki (JP 05053857 A)

See Paper No. 8 for detailed action of prior rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-17, 22, 23, 27, 29 and 32-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama, Hideki (JP 05053857 A).

See Paper No. 8 for detailed action of prior rejections.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
April 5, 2003

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100